

6 depositing a photoresist layer on the insulation layer;  
A1 7 Sub 1 exposing and developing the photoresist layer for providing a photoresist mask pattern for  
cont. 8 subsequent etching of the insulation layer; and  
9 removing the fill-in material from the aperture.

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1 11. (Once Amended) In an integrated circuit manufactured using a via-first dual damascene  
2 process and having a low-K dielectric material as an insulation layer on a wafer substrate, a  
3 photolithographic pattern comprising:  
Sub 1 4 an aperture etched into an insulation layer on a wafer substrate filled with a fill-in material  
5 for isolating the insulation layer from photoresist deposited thereafter; and  
6 a photoresist layer deposited on the insulation layer, in which the photoresist layer is  
A2 7 exposed and developed for providing a photoresist mask pattern for subsequent etching of the  
8 insulation layer  
9 wherein the fill-in material is removed after the photoresist mask pattern is formed.

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1 12. (Once Amended) The pattern as in claim 11, wherein the aperture is fully filled and  
2 thereafter removed.

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A3 1 Sub 1 16. (Once Amended) The pattern as in claim 11, wherein the aperture is partially filled and  
2 thereafter removed.

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A marked up version of the amended claims, showing the changes by underlining of the added text and bracketing of the deleted text, is appended hereto.